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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/616,114	07/09/2003	Thomas Hanuschek	P2002,0587	2189

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EXAMINER	
TRUONG, LOAN	
ART UNIT	**PAPER NUMBER**
2114	

DATE MAILED: 03/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/616,114	HANUSCHEK ET AL.	
	Examiner	Art Unit	
	LOAN TRUONG	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *7/9/2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1-6 are rejected under 35 U.S.C. 102(b) as being anticipated by Krishna et al. (US 6,000,048).

In regard to claim 1, Krishna et al. disclosed an integrated module, comprising:

an external access terminal (*PCI bus, fig. 2, 12, col. 5 lines 23-27)*;

a memory for storing code and data (*8-bit test register provides control information and receives testing result, fig. 3, 92, col. 5 lines 61-67 and col. 6 lines 1-15)*;

a microcontroller (*BIST control unit, fig. 2, 78, col. 5 lines 43-48)* connected (*BIST circuitry connects to VLSI tester or host computer through the PCI bus, fig. 2, 12, col. 5 lines 23-27)* to said external access terminal (*PCI bus, fig. 2, 12, col. 5 lines 23-27)* and to said memory (*8-bit test register, fig. 3, 92, col. 5 lines 61-67 and col. 6 lines 1-15)*, said microcontroller (*BIST control unit, fig. 2, 78, col. 5 lines 43-48)* controlling an access (*reading control information and write testing results, col. 5 lines 61-67 and col. 6 lines 1-15)* to said memory (*8-bit test register, fig. 3, 92, col. 5 lines 61-67 and col. 6 lines 1-15)* and a data transfer (*PCI bus rewrite to any DRAM or SRAM or register in BIST non-testing phase, col. 6 lines 23-27)* through said external access terminal (*PCI bus, fig. 2, 12, col. 5 lines 23-27)* during normal operation (*operation when*

BIST is not in testing mode, col. 6 lines 23-27), said microcontroller (*BIST control unit, fig. 2, 78, col. 5 lines 43-48)* controlling a performance of a test sequence (*256 instruction to be executed by the BIST microcontroller, col. 4 lines 58-67 and col. 5 lines 1-3)* for functional testing said memory (*memory testing, col. 4 lines 58-62)* in a test operation of the module (*BIST operations, col. 4 lines 50-57)*; and

a defect data memory for storing defect data (*8-bit test register receives testing result, fig. 3, 92, col. 5 lines 61-67 and col. 6 lines 1-15)* under control of said microcontroller (*BIST control unit, fig. 2, 78, col. 5 lines 43-48)*, the defect data (*8-bit test register receives testing result, fig. 3, 92, col. 5 lines 61-67 and col. 6 lines 1-15)* being generated during the functional testing (*self test results are stored in test register, fig. 2, 92, col. 5 lines 61-67 and col. 6 lines 1-15).*

In regard to claim 2, Krishna et al. disclosed the integrated module according to claim 1, further comprising a command memory (*palette SRAM, fig. 2, 26, col. 5 lines 4-11)* for storing an externally supplied command sequence (*BIST program read from the VLSI tester, col. 5 lines 4-11)* and on a basis of the command sequence said microcontroller controls a carrying out of the test sequence (*BIST control unit cycle through an instruction RAM, fig. 2, 58, 78, 26, col. 5 lines 51-60).*

In regard to claim 3, Krishna et al. disclosed the integrated module according to claim 1, wherein said defect data memory (*8-bit test register receives testing result, fig. 3, 92, col. 5 lines 61-67 and col. 6 lines 1-15)* is part of said microcontroller (*combine logic/BIST section, fig. 3,*

54, col. 5 lines 38-40).

In regard to claim 4, Krishna et al. disclosed the integrated module according to claim 2, wherein said command memory (*8-bit test register provides control information, fig. 3, 92, col. 5 lines 61-67 and col. 6 lines 1-15)* is part of said microcontroller (*combine logic/BIST section, fig. 3, 54, col. 5 lines 38-40).*

In regard to claim 5, Krishna et al. disclosed a method for functionally checking a memory of an integrated module, which comprises the steps of:

reading-in (*load test program into SRAM, fig. 4, 102)* a command sequence (*palette SRAM, fig. 2, 26, col. 5 lines 4-11)* externally (*BIST program read from the VLSI tester, col. 5 lines 4-11)* before beginning a test operation (*Set start, fig. 4, 104)*, and on a basis of the command sequence (*BIST control unit cycle through an instruction RAM, fig. 2, 58, 78, 26, col. 5 lines 51-60)* a microcontroller controls (*BIST control unit, fig. 2, 78, col. 5 lines 43-48)* a carrying out of a test sequence (*testing, fig. 4, 106)*;

executing the command sequence (*palette SRAM, fig. 2, 26, col. 5 lines 4-11)* for carrying out the test sequence (*256 instruction to be executed by the BIST microcontroller, col. 4 lines 58-67 and col. 5 lines 1-3)* by the microcontroller (*BIST control unit cycle through an instruction RAM, fig. 2, 58, 78, 26, col. 5 lines 51-60)*; and

storing defect data in a defect data memory (*store the results of the self test in the test register, fig. 2, 92, col. 5 lines 65-67 and col. 6 lines 1-15)* under the control of the

microcontroller (*BIST control unit, fig. 2, 78, col. 5 lines 60-67).*

In regard to claim 6, Krishna et al. disclosed the method according to claim 5, which further comprises:

making a jump (*JUMPX, JUMPY and GOTO operations, col. 7 lines 60-67 Table 3 and Table 5)* to a start address in an internal command memory (*8-bit test register provides control information, fig. 3, 92, col. 5 lines 61-67 and col. 6 lines 1-15)* after the command sequence (*BIST control unit cycle through an instruction RAM, fig. 2, 58, 78, 26, col. 5 lines 51-60)* is read-in at the beginning (*load test program into SRAM, fig. 4, 102)* of the test operation (*Set start, fig. 4, 104)*;

executing the command sequence (*palette SRAM, fig. 2, 26, col. 5 lines 4-11)* under the control of the microcontroller (*BIST control unit cycle through an instruction RAM, fig. 2, 58, 78, 26, col. 5 lines 51-60)* proceeding from the start address (*start from the first instruction in the 256 18-bit instruction stored in SRAM, fig. 4, 26, col. 6 lines 52-54)*; and

storing the defect data generated in the defect data memory (*store the results of the self test in the test register, fig. 2, 92, col. 5 lines 65-67 and col. 6 lines 1-15)* under the control of the microcontroller (*BIST control unit, fig. 2, 78, col. 5 lines 60-67)*; and

reading-out (*VLSI tester reads from test register, fig. 4, 110, col. 65-67)* the defect data stored in the defect data memory (*8-bit test register receives testing result, fig. 3, 92, col. 5 lines 61-67 and col. 6 lines 1-15)*, under the control of the microcontroller (*BIST control unit, fig. 2, 78, col. 6 lines 64-67)*, to outside the integrated module for further evaluation (*VLSI tester or host computer, fig. 2, 66, 10).*

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See PTO 892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Loan Truong whose telephone number is (571) 272-2572. The examiner can normally be reached on M-F from 8am-4pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571) 272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Loan Truong
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